I CLAIM:

1. A network interface suitable for receiving frame data over a network, comprising:

a media access control providing a connection to a media interface;

a buffer manager operationally coupled with the media access control and configured to receive frame data from the media access control; and

a memory operationally coupled with the buffer manager wherein the buffer manager is configured to write the frame data to the memory.

2. The network interface of claim 1, wherein the memory comprises a dual port memory.

3. The network interface of claim 1, wherein the memory is partitioned into a plurality of segments.

4. The network interface of claim 1, wherein the media access control is configured to receive ethernet frame data from the media interface.

5. The network interface of claim 1, wherein the media access control is configured to filter incoming frame data.

6. The network interface of claim 5, wherein the media access control is configured to detect repetitions of a pre-defined address.

7. The network interface of claim 5, wherein the media access control performs error detection and provides error signals to the buffer manager.

8. The network interface of claim 3, wherein the buffer manager comprises an index pointer selecting one of the memory segments.

9. The network interface of claim 3, wherein the buffer manager generates an overflow signal if an incoming frame exceeds the length of a memory segment.

10. The network interface of claim 3, wherein the buffer manager generates a lost packet signal if incoming frame data is received while all of the memory segments contain unread frame data.

11. The network interface of claim 1, wherein the buffer memory comprises a random access memory.

12. The network interface of claim 3, wherein the buffer memory provides simultaneous access for writing frame data to a first memory segment of the plurality of memory segments and for reading frame data from a second memory segment of the plurality of memory segments.

13. The network interface of claim 12, wherein the buffer memory comprises a circular memory buffer.

14. A method for operating a receive buffer memory having a plurality of segments, comprising the steps of:

receiving first and second frame data from a network;

writing the first frame data to a first segment of the receive buffer memory;

writing the second frame data to a second segment of the receive buffer memory; and

reading the first frame data from the first segment of the receive buffer memory simultaneous to the step of writing the second frame data.

15. The method of claim 14, wherein the step of receiving first and second frame data further comprises receiving a plurality of words for each of the first and second frame data.

16. The method of claim 15, wherein the steps of writing the frame data further comprise writing the plurality of words to sequential addresses within the first and second segments.

17. The method of claim 14, wherein the step of reading the first frame data comprises reading a plurality of words from sequential addresses within the first segment.

18. The method of claim 14, further comprising the step of generating an overflow signal when the first frame data exceeds the capacity of the first memory segment.

19. The method of claim 18, wherein the step of writing the first frame data comprises writing only a first portion of the first frame data to the first segment.

20. The method of claim 14, further comprising the steps of:

receiving additional frame data for a plurality of frames; and

writing the additional frame data to memory segments in the buffer memory only if the memory segments have been read.

21. The method of claim 20, further comprising the step of generating a lost packet signal if all of the plurality of segments contain unread frame data.

22. A controller suitable for monitoring events related to a computer system, comprising:

a control processor configured to communicate with a host processor;

a plurality of connections operationally coupled with the control processor, wherein the control processor is configured to monitor system events over the plurality of connections; and

a network interface operationally coupled with the control processor and having a memory, wherein the memory provides frame data to the control processor, and wherein the control processor is configured to monitor network events from the frame data.

23. The controller of claim 22, wherein the memory comprises a dual port memory.

24. The controller of claim 22, wherein the control processor comprises a processor having an Industry Standard Architecture bus connection.

25. The controller of claim 22, wherein the plurality of connections comprise:

a fan speed connection;

a plurality of voltage connections; and

a plurality of temperature connections.

26. The controller of claim 22, wherein the memory is partitioned into a plurality of segments and each of the segments are sized to hold a single frame.

27. The controller of claim 26, wherein the network interface further comprises:

a media access control providing connections to a media interface; and

a buffer manager operationally coupled with the media access control and the memory, wherein the buffer manager receives frame data from the media access control and writes the frame data to the memory.

28. The controller of claim 27, wherein the buffer manager is configured to write frame data relating to a single frame in only one of the plurality of segments.

29. The controller of claim 28, wherein the buffer manager is configured to generate an overflow signal if the frame data does not fit within a segment.

30. The controller of claim 28, wherein the buffer manager is configured to generate an overflow signal if each of the plurality of segments contain unread frame data.

31. The controller of claim 28, wherein the memory comprises a circular memory.

32. The controller of claim 31, wherein the memory is configured simultaneously to provide frame data from one segment of the plurality of segments to the control processor and writes frame data to another segment.

33. The controller of claim 27, wherein the network interface comprises an ethernet interface.

34. The controller of claim 22, further comprising an isolation connection, wherein the controller provides a signal over the isolation connection to isolate a host media access control from the media interface.

35. The controller of claim 22, wherein the memory comprises a random access memory.

36. A method for operating a computer system of the type having a network connection, comprising the steps of:

entering a reduced power state;

receiving a plurality of frames from a network;

filtering the plurality of frames;

writing first frame data from the plurality of frames to a first segment of a receive buffer memory; and

reading the first frame data from the first segment of the receive buffer memory.

37. The method of claim 36, wherein the step of entering a reduced power state comprises disabling a host processor.

38. The method of claim 36, wherein the step of receiving a plurality of frames comprises receiving a plurality of words, wherein the plurality of words contain data relating to the plurality of frames.

39. The method of claim 36, wherein the step of filtering the plurality of frames comprises filtering based upon a destination address field.

40. The method of claim 36, wherein the step of filtering the plurality of frames comprises filtering based upon a predefined bit pattern.

41. The method of claim 36, wherein the step of filtering the plurality of frames comprises filtering based upon detection of repetitions of a destination address.

42. The method of claim 36, wherein the step of writing first frame data comprises writing a plurality of words to a random access memory, wherein the plurality of words contain data relating to the first frame.

43. The method of claim 42, wherein the step of reading the first frame comprises reading the plurality of words.

44. The method of claim 36, further comprising the step of generating an overflow signal if the size of the first frame data exceeds the size of the first segment.

45. The method of claim 36, further comprising the step of writing second frame data to a second segment of the receive buffer memory wherein the step of reading the first frame data occurs simultaneous to the step of writing the second frame data.